Nano-Power and High-Q CMOS Differential Active Inductor in Weak Inversion except the high-Q in strong inversion

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Abstract—This paper presents a novel 2-port high-Q differential active inductor in weak inversion and strong inversionDAI(WI, SI) using negative impedance circuit. The proposed 2-port high Q differential active inductor DAI(WI,SI) consists of the feedback parallel resonance circuits that comprises of negative impedance circuit and differential gyrator for stabilizer . The novelty of the proposed structure can improve its Q-factor due to decrease ofthe Parasitic capacitances, series resistance and extend high power dissipation is in strong inversion except low inweak inversion. For an experimental validation, the 2- port differential active inductor DAI(WI ,SI) was fabricatedwithin 130 nm BSIM3V3 CMOS technology. The fabricated circuit in weak inversion shows inductance L in theneighborhood of value 1263000 nH and quality factor Q to the value approach 1711 in the frequency range of 0.119-0.3598GHz for strong inverting product inductance L in the neighborhood of value 1420nH and quality factor Qto the value approach 1698 in the frequency range of 1.45000010 -1.45000045GHz.

1 Introduction

There are many uses for inductors, especially forfilters, RF chokes, and magnetic storage devices forL-C tanks. Inductors are useful because their electronic behavior is complimentary to capacitors sincetheir impedance increases with frequency[1-3].Withreal inductors implemented using coiled wires[4-6],theimpedance increases with frequency till the selfresonance frequency (SRF) is reached after which theinductor no longer behaves like an inductor[7,8],butlike a capacitor .An ideal gyrator is a linear two portnetwork that neither stores nor dissipates energy[9].Onchip passive inductors exhibit poor quality-factor[5] and require large silicon die area. The circuit has a lowpower consumption[10].The circuit is suitable for implementing high qualityfactor of the DAI in multi-standard applications suchas a wireless communication system. A wide-rangetunable CMOS AI based on a cross-coupled pair oftransistors providing positive feedback for enhanced Q factor, and high resonance frequency ω_0 has been reported [11] Applications of the active inductor includeWilkinson power divider [12], phase shifter [13], filter [14], [15], oscillator [15], and current-mode phaselocked loop [16].A differential inductor is a mandatorycomponent in these differential circuits.We have proposed a compact source-degenerated differential active inductor in [17]. Our proposed differential active inductors utilize only two MOSFETs forthe necessary differential gyrator, compared to a conventional differential active inductor (DAI) that usuallyrequires four MOSFETs [15]. Unfortunately the DAIdemonstrated in [17] does not exhibit high-Q for frequencies more than 1 GHzIn this letter, the high frequency of the DAI based on[17] has been improved. Since current-controlled inductance is desired for most applications, a replica biascircuit has been introduced for the new DAI.This paper is organized as follows. Section II discussesabout basic floating gyrator- C the proposed active inductor in strong inversion followed by simulation

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results Section III introduces proposed active inductor inweak inversion followed by simulation results and conclusion in section IV.

2 Proposed And Improved DAI CircuitDesign in Strong Inversion(SI).

All transistors are operated in the saturation region.

2.1 Quality factor of an oscillator

The quality factor (Q-factor) is one of the major important performance determining characteristic of anyresonant circuit. It is the measure of the ideality of thereactive components of the resonant circuit. There aredifferent means to define Q-factor [18] of a system. Inbasic physics it is defined as

$$Q = 2\pi * \frac{EnergyStored}{EnergyDissipated} * PerCycle \quad Or \quad Q = \frac{imag(Z_{in})}{real(Z_{in})} \tag{1}$$

With

$$Z_{in} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \tag{2}$$

A resonance occurs when the peak magnetic energy equals the peak electric energy $X_c = -X_L$ where C is the Total circuit capacitance, and the resonant frequency is $f_{srf} = \frac{1}{2\pi\sqrt{LC}}(Hz)$

In this case and beyond the self-resonant frequency, no net magnetic energy is available [18]

$$L = \frac{imag(Z_{in})}{2\pi f} \quad is \quad inductance \tag{3}$$

$$L = \frac{1}{2\pi f\, imag(Z_{in})} \quad is \quad capacitor \tag{4}$$

2.2 The MOS Transistor the strong inversion (SI) regim saturation.

2.2.1 Large and tunable quality factor

The quality factor of CMOS active inductors is defined with the ohmic loss of the inductors, arising essentially from the finite output resistance of the transconductors of the inductors .In fact ,the Quality factor of CMOS active inductor (AI) can be maximized through the increase of the output Resistance [19]. There are several strategies to increase the output resistance.Just as an example negative resistor compensation, and were designed for $0.13\mu m$ CMOS technology using BSIM3V3 models, simulated with Cadence software, with the following parameters:

$$\mu C_{ox} = 500\frac{\mu A}{V^2}, \quad V_{TH} = 0.62V, \quad C_{ox} = 12.3\frac{fF}{\mu m^2} \tag{5}$$

The circuits were designed for the power supply voltage $V_{DD} = 3.3V$ and $C_{gs} = \frac{2}{3}C_{ox}WL$. The base element of a CMOS circuit is the MOSFET transistor [20].

Considering the saturation region the drain current produced by the NMOS transistor is approximately given by Equation(6):

$$I_{ds} = I_D = K_{N/P}\frac{1}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda v_{ds}) \tag{6}$$

where k is the mobility constant and it is a technology parameter (K_P refers to PMOS transistors and K_N refers to NMOS transistors),W is the width of the transistor, L is the length of the transistor,V_{GS} is the gate-to-source voltage drop, $V_{GS} - V_{TH} = V_{DS_{sat}}$ and V_{TH} is the threshold voltage (transistor operating voltage).

In this region the drain current is weakly dependent upon drain voltage and it is controlled essentially by the gate-source voltage (considering small variations of the threshold voltage). Considering the facts aforementioned, it is possible to obtain the current (I)-voltage (V) characteristic of the transistor and define the MOSFET transconductance given by Equation (7) which is a current gain and a key design parameter for a transistor [21].

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{7}$$

To prevent parasitic coupling , the bulk must be at the same voltage potential as the source in a NMOS transistor and the same voltage potential as the drain in a PMOS transistor. Nevertheless, this is not always guaranteed .Considering the NMOS case the body effect describes how much the threshold voltage is affected by the change in the

source-bulk voltage. This effect, expressed in a constant γ, is expected in differential pairs and diode connected NMOS [21].The small signal linear model for the saturation region with short channel ($\lambda \propto \frac{1}{L}$) is showed in the Fig.1. This figure (Fig.1) shows the AC small-signal model of the MOSFET in strong inversion with both small signal transconductances included. Small Signal characteristics (Low-frequency). The Equation (8) relates the body effect

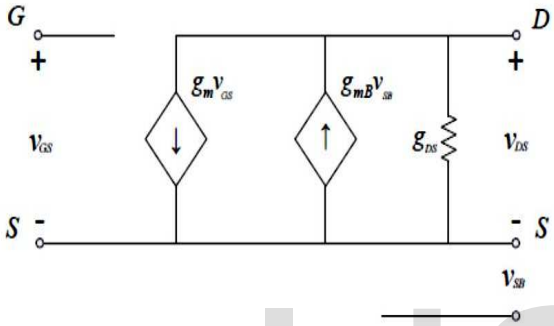

Fig. 1. WSmall-signal MOSFET with both transconductances.

and threshold voltage:

$$\Delta V_{TH} = \gamma(\sqrt{2 \mid \phi_p \mid + V_{sb}} - \sqrt{2 \mid \phi_p \mid}) \tag{8}$$

ϕ_p is the surface potential parameter and V_{sb} is the source to bulk voltage. This effect leads to the appearance of an extra transconductance term (Equation (9))

$$g_{mb} = -\frac{\partial I_D}{\partial V_{sb}}(Equation(9),\ with\ constant\ V_{ds},\ V_{gs}) \tag{9}$$

$g_{mb} = -\frac{\gamma}{2\sqrt{2|\phi_p|+V_{sb}}} g_m = \frac{C_S}{C_{OX}} g_m = \eta g_m$, with $0.1 \leq \eta \leq 0.3$. If we call the transition frequency where the current gain of the MOSFET is one .The transition frequency, f_T (the transistor transitions from an amplifier to an attenuator) and we remember that $C_{gs}(= \frac{2}{3} W L C_{OX}) \gg C_{gd}$, $V_{GS} - V_{TH} = V_{DS_{sat}}$ Then we can write

$$1 = |\frac{i_d}{i_g} \approx \frac{g_m}{2\pi f(c_{gs})} \longleftrightarrow f_T \approx \frac{g_m}{2\pi(c_{gs})} = \frac{4\mu_n}{4\pi} * \frac{V_{DS_{sat}}}{L^2} \tag{10}$$

This equation is fundamentally important. Fig. 2(a) shows

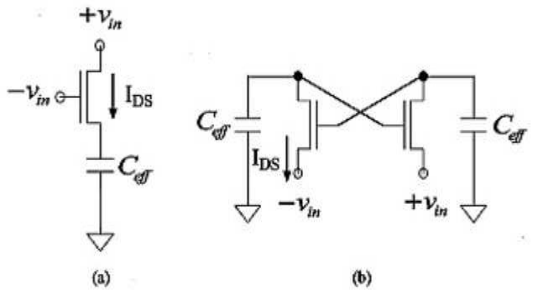

Fig. 2. Simple gyrator with input ports at gate and drain and (b) simple gyrator with input ports at source.

the basic idea of the DAI in given [17] whereas Fig. 2(b) shows the new improved DAI with input at the source. Operation of both DAIs can be explained as follows. When an input signal of opposing sign($\mp v_{in}$) is applied simultaneously to the gate and drain (or source for Fig. 2(b)) of the MOSFET respectively, a simple gyrator is formed. The input port is inductive when a capacitor terminates the second port of the gyrator ,as shown in Fig. 2. Assuming that the operating frequency is much lower than MOSFET's cut-off frequency $f \ll \frac{g_m}{(2\pi C_{gs})}$ and ignoring MOSFFET output admittance (g_{ds})and C_{db} then the input admittance of Fig. 2 can be derived as follows:

$$Y_{in}(s) \approx +sC_1 - kg_m + \frac{g_m^2}{kg_m + sC_{eff}} \tag{11}$$

where k equals $+1$ and -1 in Fig.2(a) and Fig.2(b) respectively, g_m is the MOSFET transconductance, C_1 and C_{eff} and represent effective capacitance at input port and second port of the gyrator, respectively. Since input signals of opposing signs are required for the simple gyrators shown in Fig. 2, they are by nature Differential circuits. However $\pm g_m$, terms appear in (11), suggesting the proposed gyrator structure may not be stable and may experience high losses. To overcome these problems, a pair of stabilizers (M_{3a} and M_{3b}) and a negative impedance cross-coupled MOSFET pair (M_{2a} and M_{2b} have been included at the drain

and source of the proposed gyrator circuit respectively, as shown in Fig.3. No extra current dissipation penalty occurs since all the structures share the same current flow. The

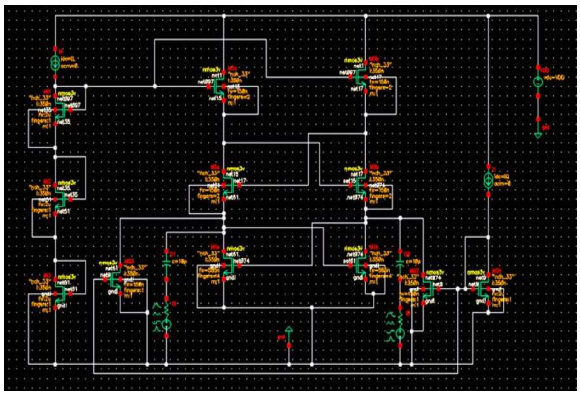

Fig. 3. Improved DAI with current-controlled inductance and Q

impedance transformation (i.e. from capacitive loading to inductive loading) can be derived with small signal models of the above circuit and Kirchhoff's Current Law as follows:

$$Y_{in}(s) \approx 2(sC_1 + g_1 + g_{m2} - g_{m1} + \frac{g_{m2}^2}{sC_2 + g_2 + g_{m3} - g_{m2}}) \quad (12)$$

$$\frac{1}{R_S} = \frac{g_{m2}^2}{g_2 + g_{m3} - g_{m2}}, \quad G_p = 2g_1 + 2g_{m2} - 2g_{m1} \quad (13)$$

$$L = \frac{C_2}{2g_{m2}^2}, \quad C_p = 2C_1 \quad (14)$$

$$Y_{in}(s) \approx (sC_p + G_p + \frac{1}{sL + R_S}) \quad (15)$$

where C_1, C_2 and g_1, g_2 are the effective parasitic capacitance and conductance at node 1 and 2 respectively. Equation (12) would suggest that by choosing a proper value for g_m , the Q of the proposed DAI theoretically can be infinite. Unfortunately Q is highly influenced by process variation and inductance tuning.

In equation (12), the parallel capacitance C_1 can be reduced by feedback negative impedance resonator which can be increased the bandwidth.

The Q-factor of an inductor is defined as the ratio of energy stored in the inductor to power loss during one cycle. Hence external flexible Q tuning is necessary. This can be implemented by increasing the value g_{m1} of so that $g_{m1} > g_{m2}$ and introducing a pair of current sinks M_Q as shown in Fig. 3. External Q tuning can be performed by varying I_Q which leads to changes in g_{m1}. Note that Q tuning will only change g_{m1} while keeping g_{m2} almost constant since only current flowing in M_1 is varied. Q tuning is almost orthogonal with inductance tuning for this DAI. Note also that only resistance loss at input can be cancelled via external Q tuning. If the DAI in Fig. 2(a) is chosen, only series resistance loss that dominates at low-frequency can be cancelled through external Q tuning [17]. This explains why the DAI demonstrated in [17] does not exhibit high Q at high frequency. On the other hand, if the DAI in Fig.2(b) is chosen, parallel resistance loss that dominates at high-frequency can be reduced by external Q tuning and this increases the DAI's Q at high frequency. Since in most cases current controlled inductance is required for a DAI, a replica of one branch of the DAI is used as a current mirror that controls current flow in the DAI, as shown in Fig.3. The Q factor of the proposed active inductor in Fig.3 can be given as (16):

$$Q = (\frac{\omega L}{R_S}) \frac{1}{1 + R_S G_p [1 + (\frac{\omega L}{R_S})^2]}$$
$$with \quad \frac{1}{R_S} = \frac{g_{m2}^2}{g_2 + g_{m3} - g_{m2}} \; G_p = 2g_1 + 2g_{m2} - 2g_{m1} \quad (16)$$

As shown in (16), the Q-factor of active inductor can improved by minimizing R_s. To realize smaller series resistance R_s and maintain high inductance, the series resistance should be as small as possible by optimizing circuit parameters. As seen from (16), the R_s can be reduced by increase the g_{m2}, which results in the improvement of the Q-factor of the active inductor. Also we should choose the small g_m so that the G_p can be reduced.

A current-regulated DAI gives better process variation control compared to voltage-regulated DAI.

2.3 Experimental Results

The proposed circuit was fabricated using 130 nm BSIM3V3 CMOS process. The simulation was performed in Cadence Spectre by using SP simulation. The transistor sizes used

TABLE 1

device size of the proposed DAI in strong inversion .

Transistors	size(um/um)	Fingers
M1a M1b	*2.34/0.35*	*4*
M2a M2b	*0.3/0.35*	*2*
M3a M3b	*0.3/0.35*	*2*
MQ1	*2/0.35*	*1*
MQ2 MQ3	*0.15/0.35*	*1*
Mi3 Mi2 Mi1	*2/0.35*	*1*

for the DAI are shown in Table 1. The proposed circuit consumes $107.976\ mW$ DC power at 3.3 V supply voltage. Fig.4 shows the simulated inductances L and Q-factors of the DAI circuit.

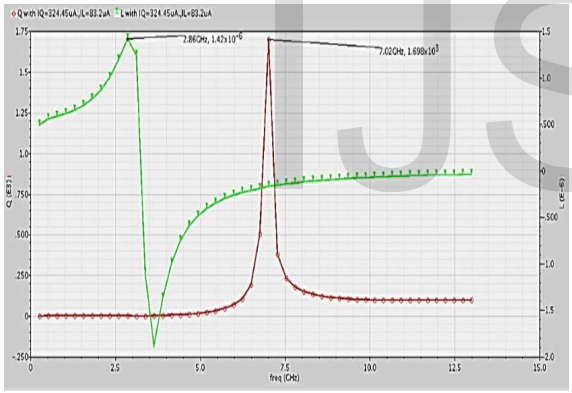

Fig. 4. Shows the simulated inductances L and Q-factors of the DAI circuit.with $IL = 83.2\mu A$, $IQ = 324.45\mu A$.

The maximum inductance is $1420nH$ at low frequency and maximum Q-factor is 1698 at $7.02GHz$. DAI resonance at $3.5GHz$. Fig.5 shows the relationship between L, resonance frequency f0, and IL tuning. Maximum to minimum L ratio is around 9 while the DAI circuit core dissipates power not more than $1.557mW$. As mentioned before, Q tuning of the proposed DAI is nearly orthogonal with L, as shown in Fig.6. Possible achievable $Qmax$ depends on IL and minimum resolution of IQ ,where IQ is varied.

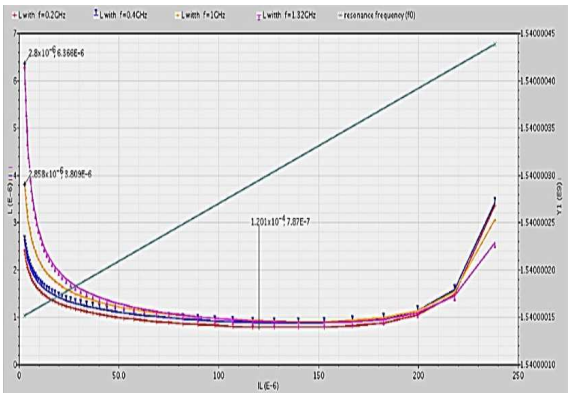

Fig. 5. Relationship between L, resonance frequency f_0, and IL tuning of the new DAI.

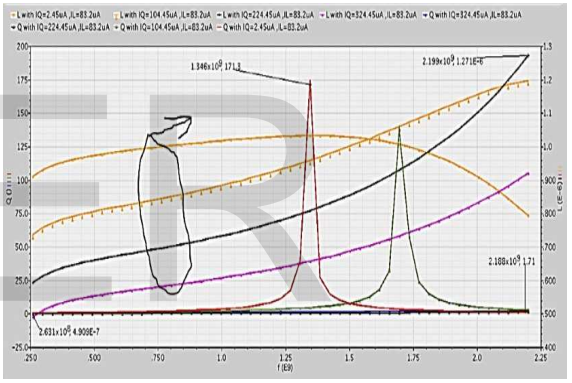

Fig. 6. Flexible Q tuning is almost orthogonal with inductance L. $IL = 83.2\mu A$. IQ varied from $2.45\mu A$ to $224.45\mu A$.

3 Proposed and Improved DAI Circuit Design in Weak Inversion(WI)

We show that the gyrator-C synthesized active inductors hold when the transistors of the gyrators are in weak inversion. Fig.7 shows Improved DAI with current-controlled inductance and Q in weak inversion. In this section, we use active inductor proposed in reference [17] to develop active inductor in sub-threshold. By adjusting the current of the all transistors, these parameters and subsequently the resonant frequency and quality factor of the active inductor can be varied. Having analyzed differential active induc-

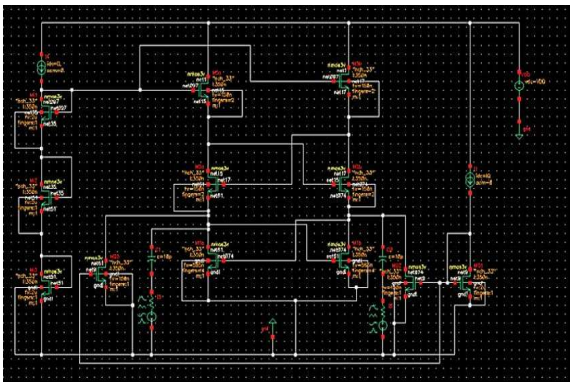

Fig. 7. Improved DAI with current-controlled inductance and Q.

tor in strong inversion, we now turn out attention to active inductors in subthreshold. In the sub-threshold region, the channel current is mainly due to the diffusion of minority charge carriers in the channel, and is much smaller as compared with that in the saturation region. The MOS Transistor in Weak Inversion (WI):

In this section we will explore the behavior of the MOS transistor in the subthreshold regime where μ the channel is weakly inverted. This will allow us to model transistors operating with small gate voltages, where the strong inversion model erroneously predicts zero current. The expression (17) for drain current in a subthreshold MOSFET [22]:

Drain current I_D:

$$I_D = I_{D_0} * \frac{W}{L} * exp^{(\frac{V_{gs}}{nV_t})} * (1 - exp^{(\frac{-V_{ds}}{V_t})}) \tag{17}$$

With

$$V_t = \frac{k*T}{q} \cong 26mV \quad at \quad T = 300K, \\ n = \frac{C_{OX}+C_{dep}}{C_{OX}} \cong 1.5. \tag{18}$$

And

$$I_{D_0} = \mu_n * C_{OX}(n-1) * V_t^2 * exp^{(\frac{-V_{TH}}{nV_t})} \tag{19}$$

Note: channel length modulation, i.e., λ is ignored here.

3.1 Saturation Region for Subthreshold Operation

Saturation occurs at roughly $V_{ds} > 100mV$.

$$I_D = I_{D_0} * \frac{W}{L} * exp^{(\frac{V_{gs}}{nV_t})} * (1 - exp^{(\frac{-V_{ds}}{V_t})}) \tag{20}$$

$$I_D \cong I_{D_0} * \frac{W}{L} * exp^{(\frac{V_{gs}}{nV_t})} \tag{21}$$

Assuming device is in subthreshold and in saturation:

$$I_D \cong I_{D_0} * \frac{W}{L} * exp^{(\frac{V_{gs}}{nV_t})} \tag{22}$$

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \cong I_{D_0} * \frac{W}{L} * exp^{(\frac{V_{gs}}{nV_t})} * \frac{1}{nV_t} = \frac{I_D}{nV_t} \tag{23}$$

Eq.(23) shows that the transconductance of a MOSFET in weak inversion is directly proportional to its channel current recall for strong inversion :

$$g_m = \frac{2 * I_D}{(V_{gs} - V_{TH})} \tag{24}$$

$$g_0 = \frac{\partial I_D}{\partial V_{ds}} = \frac{I_D}{V_t} \frac{(exp^{(\frac{-V_{ds}}{V_t})})}{(1 - exp^{(\frac{-V_{ds}}{V_t})})} \tag{25}$$

If $((exp^{(\frac{-V_{ds}}{V_t})}) \ll 1$, making use of
$\frac{1}{(1-exp^{(\frac{-V_{ds}}{V_t})})} \approx (1 + exp^{(\frac{-V_{ds}}{V_t})})$
we can write (25) as:

$$g_0 = \frac{\partial I_D}{\partial V_{ds}} \approx \frac{I_D}{V_t}(exp^{(\frac{-V_{ds}}{V_t})}) \tag{26}$$

Note that high-order terms are neglected in deriving (26). Since I_{ds} is small in weak inversion and $V_{ds} \gg V_t$, go in weak inversion is much smaller than that in strong inversion. The gate capacitance of MOSFETs in weak inversion is the combined effect of C_{js} and C_{OX} in series. Where C_{js} is the capacitance between gate-voltage induced depletion region and the substrate and C_{OX} is the gate-oxide capacitance.

It can be shown that the gate capacitance $C_g = C_{OX}\frac{(WL)}{3}$, where C_{OX} is gate oxide capacitance per unit area. Making use of the preceding results and (12), we obtain the inductance and parasitic series resistance of active inductor in weak inversion.

$$R_S \approx \frac{(\frac{I_{DS}}{V_t} * exp^{(\frac{-V_{ds}}{V_t})})_2 + (\frac{I_D}{nV_t})_3 - (\frac{I_D}{nV_t})_2}{2((\frac{I_D}{nV_t})_2)^2} \tag{27}$$

$$G_p \approx 2[(\frac{I_{DS}}{V_t} * exp^{(\frac{-V_{ds}}{V_t})})_2 + (\frac{I_D}{nV_t})_2 - (\frac{I_D}{nV_t})_1] \tag{28}$$

$$L \approx \frac{\frac{C_{OX}(WL)_2}{3}}{2((\frac{I_D}{nV_t})_2)^2)} \tag{29}$$

$$C_p \approx \frac{2C_{OX}(WL)_1}{3} \tag{30}$$

Eq.(27) and Eq.(29) show that increasing the currents will lower the inductance and at the same time reduce the parasitic series resistance. The former is undesirable while the latter is preferred. Clearly a compromise must be made.

3.2 Hybridy-π Model in Subthreshold Region

Looks the same in form as for strong inversion, but different expressions for the various parameters with small signal at medium frequency of the transistor NMOS as show in (Fig.8).

$$g_m \cong \frac{I_D}{nV_t}, \qquad g_{mb} \cong \frac{n-1}{n} * \frac{I_D}{V_t}, \qquad r_0 \cong \frac{1}{\lambda * I_D} \cong \frac{1}{g_{ds}} \tag{31}$$

If each transistor is modeled by the gate-source capacitance C_{gs}, transconductance g_m, the output conductance g_{ds} ($g_m >> g_{ds}$) and the gate-drain capacitance C_{gd} ($C_{gs} >> C_{gd}$) but C_{gd} and g_{ds} are neglected, then the simplified small signal equivalent circuit of the NMOS TRANSISTOR (Fig.8) may be shown as in Fig.9 and simulation as shown in Fig.10, 11a. 11b. Fig. 11a shows the drain current (I_{DS})

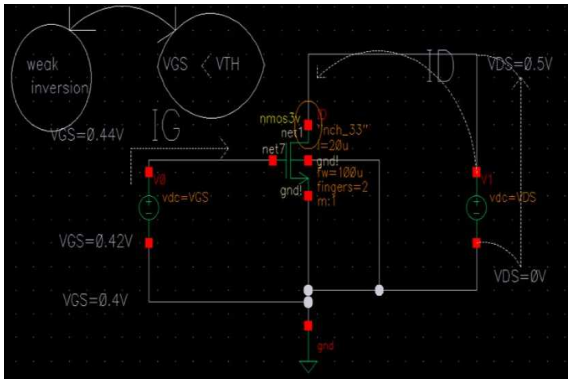

Fig. 8. NMOS transistor circuit in weak inversion.

as a function of gate source voltage (V_{GS}) for normal size transistor (width of W_1) operating in superthreshold region and relatively larger size transistor (width of $W_2 > W_1$) operating in subthreshold region. Drain current is domi-

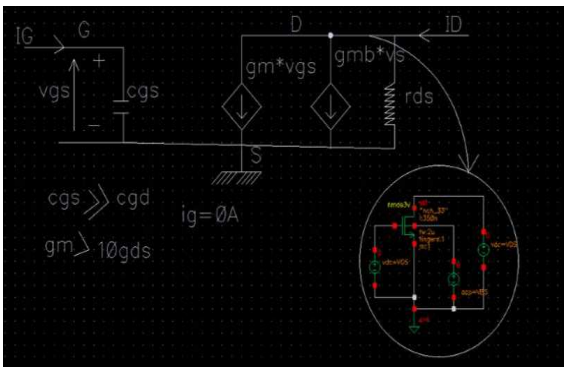

Fig. 9. Medium frequency small-signal equivalent circuit.

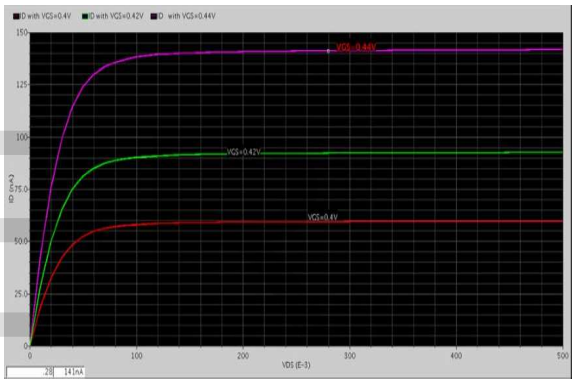

Fig. 10. Simulation the current Ids versus the voltage vds varies from $0V$ to $0.5V$ with V_{GS} append constant ($V_{GS} = 0.4V$, $V_{GS} = 0.42V$, $V_{GS} = 0.44V$

nated by drift mechanism in superthreshold region resulting in square root dependence of transconductance g_m on I_{DS}. In subthreshold region, drain current has an exponential dependence on gate voltage due to dominant diffusion mechanism resulting in a higher g_m to I_{DS} ratio of subthreshold region. Therefore, the transconductance g_m that satisfies the required differential active inductor(DAI) in subthreshold region (g_{m2}, slope at Q_2), which is equal to the transconductance g_m of the smaller transistor in superthreshold region (g_{m1}, slope at $Q1$), can be obtained at a smaller drain current (I_{DS2}). Hence, the power dissipation

of the DAI can be reduced using oversized MOS transistor operating in subthreshold design.

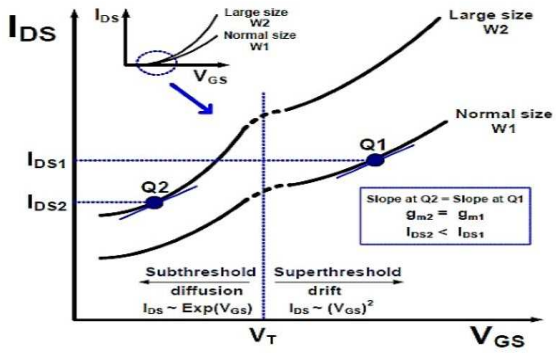

Fig. 11. Characteristic graph of the drain current (I_{DS}) versus the gate source voltage (V_{GS}) around threshold voltage for two different sized transistors

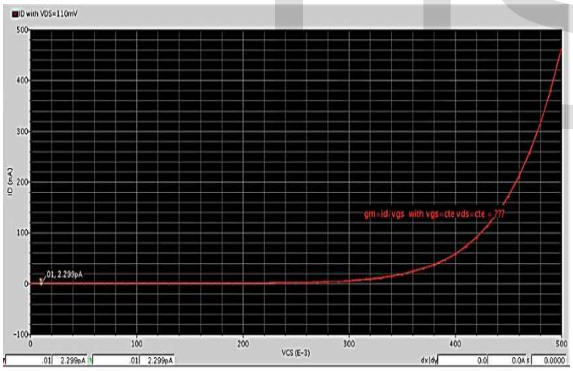

Fig. 12. Simulation of the current I_D versus the voltage V_{GS} varies at $0V$ to $0.5V$ with V_{DS} append constant ($V_{DS} = 110mV$).In weak inversion(diffusion)

3.3 experimental results

The proposed circuit was fabricated using $130nm$ BSIM3V3 CMOS process. The simulation was performed in Cadence Specter by using SP simulation. The transistor sizes used

TABLE 2
device size of the proposed DAI in weak inversion

Transistors	size(um/um)	Fingers
M1a M1b	*2.34/0.35*	*4*
M2a M2b	*0.3/0.35*	*2*
M3a M3b	*0.3/0.35*	*2*
MQ1	*2/0.35*	*1*
MQ2 MQ3	*0.15/0.35*	*1*
Mi3 Mi2 Mi1	*2/0.35*	*1*

for the DAI are shown in Table 2. The simulated inductance and parasitic Z_{in} resistance are shown in Fig.12 and Fig.13,respectively. It is seen that the synthesized inductance is much larger as compared with the corresponding active inductor in strong inversion. Also observed is that the parasitic series resistance is also much larger. The DC bias current variation IL the weak inversion of the circuit in Fig.7. were simulated with SP-parameter in Cadence Specter and the results are presented in Fig. 12. When $IQ = 10nA$, the variation trends of IL (increasing) and $VDD = 3.3V$ are consistent with the predictions of (17) and (21). The variation of IL is obviously smaller. This is because the variation of IL is alleviated by the negative resistor circuit since the circuit operates in saturation region. The measured result with maximum SRF ($359.8MHz$)

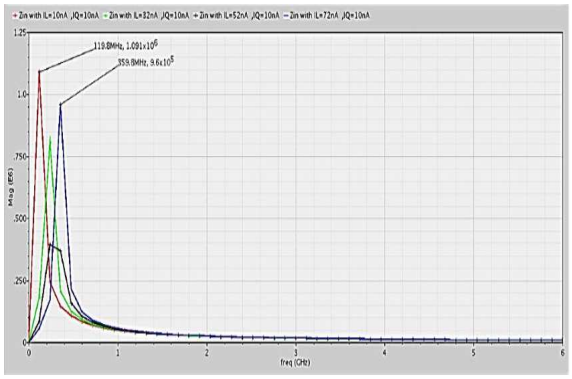

Fig. 13. Variations of Impedance Z_{in} versus the frequency (f) with DC bias current IL varies the $10nA$ to $72nA$ for $IQ = 10nA$

is shown in Fig. 12 .The maximum SRF was obtained when $IL = 72nA$ and $IQ = 10nA$. Fig.13. plots the inductance of active inductor with different biasing currents. It is seen that for the given transistor dimensions, in order to have inductance, the frequency should be below $359.8MHz$. Power dissipation of the DAI is $541.2nW$. Fig.13. demonstrates that the inductance can be tuned through IL while keeping Q almost unchanged.The maximum inductance $L(Lmax = 1263uH)$ was obtained when $IL = 10nA$ and $IQ = 10nA$ .The inductance has more than 95% tuning range frequency but The measured result with maximum Q (1711) when frequency achieves the highest value is shown in Fig. 14. As mentioned before, Q tuning

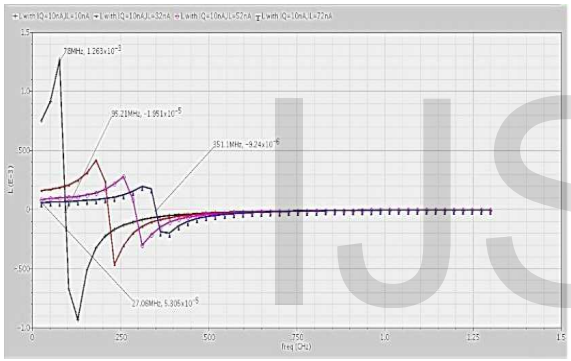

Fig. 14. Variations of inductance L versus the frequency (f) with DC bias current IL varies the $10nA$ to $72nA$ for $IQ = 10nA$

of the proposed DAI is nearly orthogonal with L, as shown in Fig.15.This figure shows that a high quality factor Q, up to 376, can be obtained while keeping SRF and L are almost unchanged with the SRF is $119MHz$.Power dissipation of the DAI is $409.2nW$. The performance comparison of the proposed CMOS differential active inductor(DAI(WI ,SI)) with state-of art is summarized in Table 3. The operating frequency of proposed circuit is lower than previous ones [23], [24], [25]. Also the proposed circuit has low power consumption and high Q factor. Moreover, although the maximum inductance ($Lmax$) is very large than previous works, the proposed circuit provides very large inductance

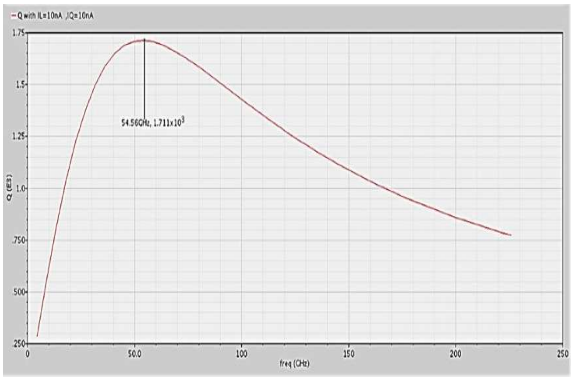

Fig. 15. Quality factor Q of the proposed DA in weak inversion versus the frequency f with $IQ = 10nA$, $IL = 10nA$

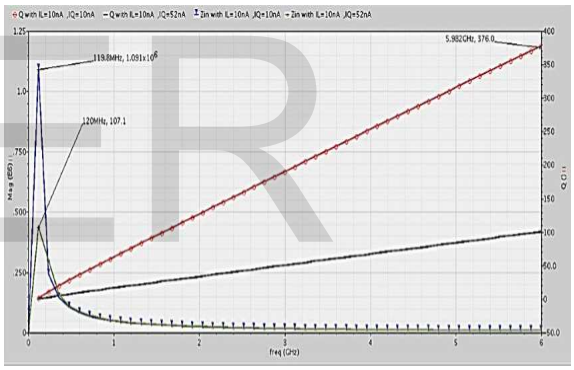

Fig. 16. Flexible Q tuning and Zin tuning are almost orthogonal with inductance L $IL = 10nA$, IQ varied from 10 to $52nA$

over the lower frequency range and can be used lower frequency Rang.

SI^* : Strong Inversion.
WI^* : Weak Inversion.
F.R: Freq. range (GHz)
Tec: Technology
Inter1=1.45000010 - 1.45000045
Inter2=0.119 - 0.3598

TABLE 3
summarized performances of this DAI (WI , SI) and its comparison with previously published data.

Items / Ref	[23]	[24]	[25]	SI^*	WI^*
Tec (nm)	180	180	180	130	130
F.R(GHz)	1 - 2	1 - 5	1 - 5	Inter1	Inter2
Lmax. (nH)	27	35	22.4	1420	1263000
Q-factor	28	68	500	1698	1711
PDC (mW)	4	3.6	4.5	107.976	0.0005412

4 Conclusion

This work presents a new differential active inductor DAI (WI,SI) whose self- resonance frequency and quality factor parameters can be adjusted independently from each other. Additionally, negative impedance cross coupled MOSFET pair (M2a,M2b) feedback is used to cancel series - loss resistance of the active inductor, which allows self- resonance frequency and quality factor enhancement as well.
The differential active inductor DAI(WI) achieves high quality factor than DAI(SI). Moreover lower power dissipating $0.5412-nW$ from a single $3.3-V$ power supply voltage in DAI(WI)is obtained while high power dissipating $107.976-mW$ from a single $3.3-V$ power supply voltage is recorded in DAI(SI).canceling parasitic components and determining the properties of the DAI independently are salient feature of the design .We believe that the enhanced linearity renders the active inductor in more practical for realizing Low-voltage, low-power RF filter for wireless applications.

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